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A Closed Form Analytical Model of Back-Gated 2-D Semiconductor Negative Capacitance Field Effect Transistors

CHUNSHENG JIANG [1,2], MENGWEI SI [2], RENRONG LIANG [1], JUN XU [1], PEIDE D. YE [2] (Fellow, IEEE), AND MUHAMMAD ASHRAFUL ALAM [2] (Fellow, IEEE)

1 Tsinghua National Laboratory for Information Science and Technology, Institute of Microelectronics, Tsinghua University, Beijing 100084, China
2 School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907, USA

CORRESPONDING AUTHORS: R. LIANG; M. A. ALAM (e-mail: liangrr@tsinghua.edu.cn; alam@purdue.edu)

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ABSTRACT Steep slope ($SS < 60$ mV/dec at room temperature) negative capacitance (NC) FETs, based on the 2-D transition metal dichalcogenide semiconductor channel materials, may have a promising future in low-power electronics because of their high on-state current and very high on/off ratio. In this paper, we develop an analytically compact drain current model for long-channel back-gated 2-D NC-FETs by solving the classical drift-diffusion equations. The equations describe the transition from depletion to accumulation regimes of operation as a continuous function of gate/drain voltages. The continuity ensures time-efficient simulation of large systems. Several key features of the model are verified by comparing with the experimental data. Specifically, the negative drain induced barrier lowering effect and negative differential resistance effect predicted by the model are successfully observed in our experiments.

INDEX TERMS Negative capacitance, two-dimensional materials, analytical model, low-power application.

I. INTRODUCTION

Recently, the excessive leakage power has been the main roadblock to further scaling of traditional MOSFETs [1], [2]. The fundamental issue is that the subthreshold swing (SS) of normal MOSFETs cannot scale below the Boltzmann's limit ($< 2.3\ k_BT/q$), even for the state-of-the-art FinFET technology. One solution involves changing carrier transport across the channel via band-to-band tunneling [3]. In 2008, Salahuddin and Datta [4] suggested a second solution: amplifying the channel potential by using the intrinsic polarization of ferroelectric (FE) materials in the gate stack, framed in the concept of a negative capacitance (NC). For initial demonstration, most experiments related to the topic have focused on the silicon (Si) NC-FETs [5]–[7]. Ultimately, however, NC-FETs must be integrated with ultra-thin body transistors for effective control of short-channel effects. Two-dimensional (2D) transition metal dichalcogenides (TMDs) have been explored as potential ultra-thin 2D channel materials for future device technology [8]. Specially, NC-FETs with MoS_2 channel material have been investigated in [9] and [10]. A steep SS has been observed over a narrow range of gate voltage, although the principle of operation of these 2D NC-FETs is not fully understood.

Recently, You and Su [11] has proposed a model for a top-gated 2D MoS_2 NC-FET. The transistor was presumed to operate in the traditional depletion-inversion regime, with a doping profile similar to that of a standard MOSFET. In practice, however, the MoS_2 transistors reported in the literature should be treated as junctionless transistors which operate in the depletion-accumulation regime. Second, the model in [11] is suitable for an idealized self-aligned top-gated transistor, but the impact/role of parasitic capacitances (C_p) has not been included. In general, the C_p is larger in the back-gated transistors reported in the literature and this capacitance has a significant impact on the capacitance matching of NC-FETs [12]. Thus, C_p plays a key role for device design of the back-gated 2D NC-FETs. Finally, the model proposed in [11] is not fully-analytical because the

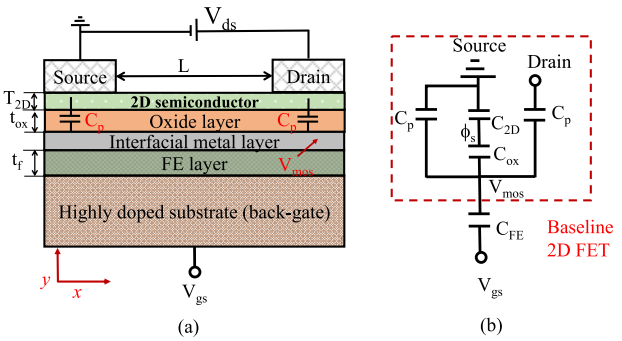

FIGURE 1. (a) Cross-section of a back-gated 2D TMD NC-FET. (b) Simplified small-signal capacitance representation of a 2D TMD NC-FET.

drain current is expressed as an implicit function of the surface potential. This implicit model may cause convergence and accuracy issues during circuit simulation [13].

In this work, we develop a fully-analytical current-voltage model to describe the electrical behavior of back-gated 2D junctionless NC-FETs. The new model can be used to optimize the device and explore its circuit implications. The paper is organized as follows. We present the detailed derivation of our model in Section II. In Section III, the proposed model is verified by the experimental data. In this section, we also investigate two important experimental phenomena of 2D NC-FETs, namely, negative differential resistance (NDR) effect and negative drain induced barrier lowering (DIBL) effect. Finally, our conclusions are summarized in Section IV.

II. MODEL DESCRIPTION

Fig. 1(a) shows the cross-section of a 2D NC-FET with a metal-ferroelectric-metal-insulator-semiconductor (MFMIS) structure. The dopant type and concentration (N_d) are presumed the same in the source, drain and channel regions. Thus, this device operates as a junctionless FET (JLT) [14]. Here, L is the gate length of the device, T_{2D} is the thickness of 2D channel, t_{ox} is the thickness of oxide layer, and t_f is the thickness of FE layer. V_{gs} and V_{ds} are the gate voltage and drain voltage, respectively. The equivalent circuit of the MFMIS gate stack is also presented in Fig. 1(b) using the simplified small-signal capacitance representation. Herein, V_{mos} is the electrostatic potential of the interfacial metal gate, and ϕ_s is the surface potential of 2D channel. C_{2D} is the 2D semiconductor channel capacitance per unit area, C_{ox} is the capacitance per unit area of the oxide layer, and C_{FE} is the capacitance per unit area of the FE layer. C_p represents the overlap and fringe capacitances between the interfacial metal gate and source/drain region. The parallel combination of C_p and C_{2D} reduces the voltage dependence of the total capacitance significantly. A relatively constant device capacitance improves capacitance matching with the ferroelectric layer, which in turn improves the overall performance of the transistor [15].

A 2D NC-FET with a MFMIS structure can be treated as a baseline 2D transistor in series with a FE capacitor [16], [17]. The electrical behavior of ferroelectric capacitor can be described by Landau-Khalatnikov equation [18]. For the baseline 2D transistor, one can obtain its transfer characteristics and output characteristics by solving the Poisson and the drift-diffusion equation.

A. MODELING OF CURRENT-VOLTAGE CHARACTERISTICS OF A BASELINE 2D FET

Electrostatic potential in the channel can be obtained by solving the Poisson equation, which can be written as,

$$\frac{\partial^2\phi}{\partial^2 x}+\frac{\partial^2\phi}{\partial^2 y}=\frac{q\,(n_{2D}-N_d)}{\epsilon_{2D}T_{2D}}$$
$$0\le x\le L, 0\le y\le T_{2D} \tag{1}$$

where $\phi(x, y)$ is the electrostatic potential in the channel, q is the electron charge, and n_{2D} is the electron density per unit area in the channel, N_d is the areal doping concentration in the channel, and ϵ_{2D} is the permittivity of 2D semiconductor. Electrons are assumed to be subject to Boltzmann law [19], so that

$$n_{2D}\approx N_{2D}\cdot exp\left[\frac{q\,(\phi\,(x,y)-V_{ch})}{k_BT}\right] \tag{2}$$

with

$$N_{2D}\equiv\frac{m^*k_BT}{2\pi\hbar^2}. \tag{3}$$

Here, N_{2D} is the effective density of states (DOS) of 2D semiconductor, and m^* is the effective electron mass. k_B is the Boltzmann constant, T is the absolute temperature, and $\hbar$ is the reduced Planck constant. The channel quasi-Fermi potential (V_{ch}) is defined by the following boundary conditions: 0 V at the source and V_{ds} at the drain. The ultrathin TMD channel consists of only a few monolayers of 2D material, therefore the electrostatic potential may be assumed uniform along the direction normal to the channel (y-direction).

As in [19], the use of Gauss's law at the interface between the 2D channel and the oxide layer transforms Eq. (1) as follows

$$\frac{d^2\phi}{dx^2}-\frac{\phi}{\lambda^2}+\xi=\frac{q(n_{2D}-N_d)}{\epsilon_{2D}T_{2D}} \tag{4}$$

where

$$\xi\equiv\frac{(V_{mos}-V_{FB0})}{\lambda^2}, \tag{5}$$

and

$$\lambda\equiv\sqrt{\frac{\epsilon_{2D}t_{ox}T_{2D}}{\epsilon_{ox}}}. \tag{6}$$

Here λ is the "natural length" for the device and ϵ_{ox} is the permittivity of oxide layer. The flat-band voltage V_{FB0} depends on the workfunction difference between the gate and the fermi-level of the 2D channel with both source/drain grounded.

A long-channel device can be described by the gradual channel approximation, that is, the electric field satisfies the condition ($E_y \gg E_x$). Therefore, Eq. (4) can be substituted into Eq. (2) to find

$$\phi(x) = V_{ch} + \frac{k_B T}{q} ln\left\{\frac{\epsilon_{2D} T_{2D}}{qN_{2D}}\left[\xi - \frac{\phi(x)}{\lambda^2}\right] + \frac{N_d}{N_{2D}}\right\} \quad (7)$$

Equation (7) can now be solved analytically using the Lambert function method, $W_0(x)$. Recalling that $W_0(x) \cdot \exp[W_0(x)] = x$, Eq. (7) can be solved as

$$\phi(x) = \frac{b}{a} - \frac{k_B T}{q} W_0\left\{\frac{q}{ak_B T} exp\left[\frac{q(b - aV_{ch})}{ak_B T}\right]\right\} \quad (8)$$

where

$$a = \frac{\epsilon_{2D} T_{2D}}{qN_{2D}\lambda^2} \quad (9)$$

$$b = \left(\frac{\epsilon_{2D} T_{2D}\xi}{q} + N_d\right)/N_{2D} \quad (10)$$

From the Pao-Sah integral current formulation [20], the drain current *vs.* voltage relationship is written as

$$\begin{aligned} I_{ds} &= \mu_n \frac{W}{L}\int_0^{V_{ds}} n_{2D} dV_{ch} \\ &= \mu_n \frac{W}{L}\int_0^{V_{ds}} \left[N_d + \frac{\epsilon_{2D} T_{2D}}{q}\left(\xi - \frac{\phi}{\lambda^2}\right)\right] d\phi \frac{dV_{ch}}{d\phi} \end{aligned} \quad (11)$$

where $dV_{ch}/d\phi$ can be found in Eq. (7). W is the gate width. At last, Eq. (11) can be expressed as a function of ϕ,

$$I_{ds} = q\mu_n \frac{W}{L}\left\{\begin{array}{c}\left[\frac{\epsilon_{2D} T_{2D}}{q}\left(\xi + \frac{k_B T}{q\lambda^2}\right) + N_d\right]\phi \\ -\frac{T_{2D}\epsilon_{2D}}{q\lambda^2}\frac{\phi^2}{2}\end{array}\right\}_{\phi_s}^{\phi_d} \quad (12)$$

Here μ_n is the effective electron mobility, which is determined by the channel doping concentration, trap density in the channel and at the interface between the 2D semiconductor channel and oxide layer, and temperature. In addition, ϕ_s and ϕ_d are calculated from Eq. (8) for ϕ by setting $V_{ch} = 0\ V$ and $V_{ch} = V_{ds}$, respectively.

B. MODELING OF CURRENT-VOLTAGE CHARACTERISTICS OF A 2D NC-FET

A completed 2D NC-FET can be treated as a baseline 2D transistor in series with a ferroelectric capacitor. Thus, according to 1D steady-state Landau-Khalatnikov equation [18], one can obtain

$$\begin{aligned} V_{gs} &= V_{mos} + V_f \\ &= V_{mos} + 2t_f \alpha Q_{av} + 4t_f \beta Q_{av}^3 + 6t_f \gamma Q_{av}^5 \end{aligned} \quad (13)$$

$$Q_{av} \equiv \frac{Q_g}{WL} = \frac{Q_{ch} + Q_{P1} + Q_{P2}}{WL} \quad (14)$$

and

$$Q_{p1} = C_p W V_{mos} \quad (15)$$

$$Q_{p2} = C_p W (V_{mos} - V_{ds}) \quad (16)$$

where the areal charge density (Q_{av}) is obtained by dividing the total gate charge (Q_g) by the transistor area ($W \times L$). In turn, Q_g is composed of three parts: intrinsic channel charges (Q_{ch}), parasitic charges at the source (Q_{P1}), and parasitic charges at the drain (Q_{P2}). These parasitic charges arise from the overlap and fringe capacitances (C_p) between the interfacial metal gate and source/drain regions as shown in Fig. 1. Note that C_p is determined by the fabrication process and the device structure. The Landau coefficients, α, β and γ, are material dependent constants; V_f is the external applied voltage across the ferroelectric layer. Once the expression of Q_{ch} is known, we can compute the electrical characteristics of the completed 2D NC-FET from Eqs. (8), (12), and (13). We will calculate Q_{ch} in the next section.

C. MODELING OF CHANNEL CHARGES OF A BASELINE 2D FET

We can calculate the channel charge (Q_{ch}) of the baseline 2D FET by using Ward-Dutton charge partitioning method [21]:

$$\begin{aligned} Q_{ch} &= qW\int_0^L (n_{2D} - N_d)\, dx \\ &= qW\int_0^L (n_{2D} - N_d)\, d\phi(x)\frac{dx}{d\phi(x)} \end{aligned} \quad (17)$$

Since the drain current is continuous at any position (x), therefore, $I_{ds}(x) = I_{ds}(L)$.Inserting this equality in Eq. (12), we find

$$\frac{x}{L} = \frac{c[\phi(x) - \phi_s] - \frac{d}{2}\left[\phi(x)^2 - \phi_s^2\right]}{c[\phi_d - \phi_s] - \frac{d}{2}\left[\phi_d^2 - \phi_s^2\right]} \quad (18)$$

where

$$c = N_d + \frac{\epsilon_{2D} T_{2D}}{q}\left(\xi + \frac{k_B T}{q\lambda^2}\right) \quad (19)$$

$$d = \frac{\epsilon_{2D} T_{2D}}{q\lambda^2} \quad (20)$$

Substituting Eq. (18) into Eq. (17) and eliminating the variable (x),

$$\begin{aligned} Q_{ch} = qWL \cdot N_{2D} &\left\{\begin{array}{c}\frac{ad}{3}\left(\phi_s^2 + \phi_s\phi_d + \phi_d^2\right) \\ -\frac{1}{2}(b_1 d + ac)(\phi_s + \phi_d) + b_1 c\end{array}\right\} \\ &/\left[c - \frac{d}{2}(\phi_s + \phi_d)\right] \end{aligned} \quad (21)$$

where a, b, c, and d are described by Eqs. (9), (10), (19) and (20), and

$$b_1 \equiv \frac{\epsilon_{2D} T_{2D}\xi}{qN_{2D}}. \quad (22)$$

III. MODEL VALIDATION AND DISCUSSION

To verify the accuracy of our model, two back-gated MoS_2 NC-FETs have been fabricated. The detailed fabrication process and device structure are described in [22]. The gate stack includes the heavily doped Si as gate electrode, 20 nm-thick $Hf_{0.5}Zr_{0.5}O_2$ (HZO) as the ferroelectric capacitor, 2 nm-thick Al_2O_3 as capping layer and capacitance matching layer. 100 nm Ni was deposited using e-beam evaporator as source/drain electrodes. The difference between

TABLE 1. Simulation parameters.

Parameters	Physical meaning	Values
L	Gate length	2 μm
T_{2D}	Thickness of MoS_2	8.6 nm (Dev.#1) 5.3 nm (Dev.#2)
t_{ox}	Thickness of Al_2O_3	2 nm
t_f	Thickness of $Hf_{0.5}Zr_{0.5}O_2$	20 nm
V_{FB0}	Flat-band voltage when V_{ds}=0 V	-0.59 V (Dev.#1) -0.56 V (Dev.#2)
C_p	Parasitic capacitance per width	3.54 fF/μm
μ_n	Effective mobility	2 $cm^2/V\cdot s$ (Dev.#1) 11 $cm^2/V\cdot s$ (Dev.#2)
N_d	Areal doping concentration	1.5×10^{12} cm^{-2}

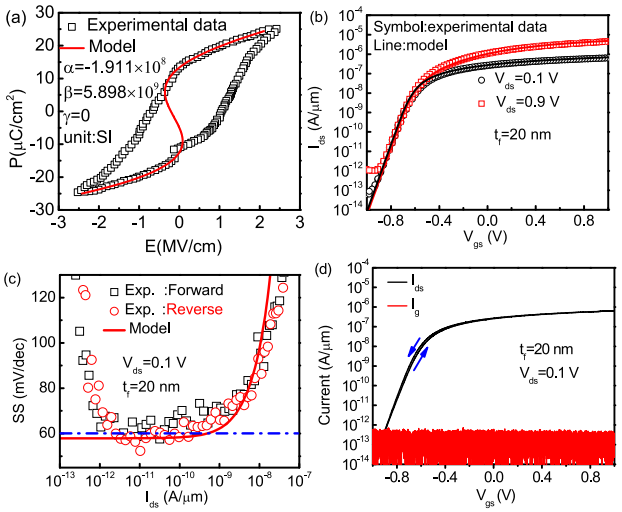

FIGURE 2. (a) Polarization vs. electric field ($P-E$) curve of $Hf_{0.5}Zr_{0.5}O_2$(HZO). $P-E$ curve is used to extract the Landau coefficients. (b) Simulated transfer characteristics of Dev. #1 for both the simulation and experiment data. (c) Subthreshold swing calculated from the transfer characteristics of the same device when $V_{ds}=0.1$ V for both the simulation and experiment measurement. (d) Gate leakage current and $I_{ds}-V_{gs}$ characteristics simultaneously measured in the Dev. #1 when $V_{ds}=0.1$ V.

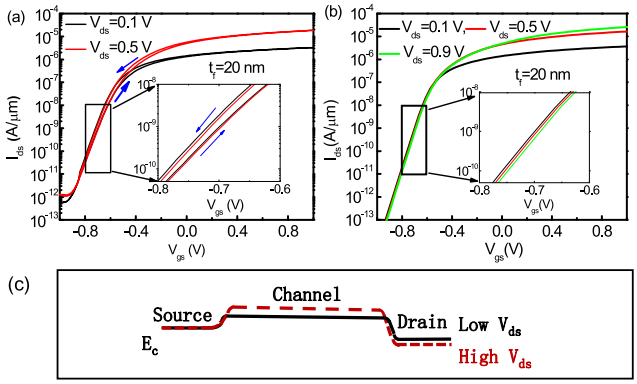

FIGURE 3. (a) Experimental transfer characteristics of Dev. #2 for different V_{ds}. (b) Simulated transfer characteristics of the same device using the model developed in this paper. (c) The conduction band energy along the channel direction when the device works in the subthreshold region.

the two devices is that they have different thicknesses of MoS_2: $T_{2D}=8.6$ nm for the first device (Dev. #1) while $T_{2D}=5.3$ nm for the second device (Dev. #2). Landau coefficients are extracted from the experimental polarization-electric field (P-E) curve as shown in Fig. 2(a). Note that our experimental measurement indicates that Schottky barrier height for source/drain contacts are insignificant at room temperature. The simulation parameters are obtained from the experimental devices shown in Table 1, unless otherwise specified.

Fig. 2(b) shows the transfer characteristics for both the simulation and experiment data of Dev. #1 for different drain voltages. Fig. 2(c) shows the subthreshold swing (SS) calculated from the transfer characteristics when $V_{ds}=0.1$V for both simulation and experiment. The hysteresis of this device is negligibly small (~12 mV). The SS is extracted for both forward sweep (SS_{For}) and reverse sweep (SS_{Rev}). Note that the device exhibits minimum $SS_{Rev}=52.3$ mV/dec, $SS_{For}=57.6$ mV/dec, which are smaller than the Boltzmann limit of 60 mV/dec. The simulated results are in good agreement with the experiment measurement, confirming the validity of the analytical model. Fig. 2(d) shows the gate leakage current and $I_{ds}-V_{gs}$ characteristics of Dev. #1 operating at $V_{ds}=0.1$ V. The pA-level gate leakage current is essentially independent of gate voltage. Thus, one can ignore the gate leakage for the following analysis.

Fig. 3 (a) shows the experimental transfer characteristics of Dev. #2 for different V_{ds}. Fig. 3(b) shows the simulated transfer characteristics of the same device using the developed model. Contrary to the normal MOSFETs, there is a "negative" drain induced barrier lowering (DIBL) effect in the transfer characteristics of the MoS_2 NC-FET as shown in Fig. 3(a) and (b). In other words, the threshold voltage of this NC-FET actually increases with V_{ds}.

It is easy to see that the negative DIBL is a consequence of the reduction of the average gate charge density per unit area. Equation (16) shows that increasing V_{ds} reduces Q_{p2}. In turn, the reduction in Q_{p2} is reflected in Q_{av} through Eq. (14). Since Q_{av} is negative for a NC-JLT in subthreshold (or depleted) region [14] and the Landau coefficient (α) is also negative by definition (the impact of β and γ can be neglected in the subthreshold regime), so that $2t_f\alpha Q_{av}$ increases with V_{ds}. Thus, Eq. (13) requires that for a given gate voltage, V_{mos} must decease when V_{ds} increases. In other words, the conduction band energy along the channel direction will be elevated when V_{ds} increases for a given gate voltage in the subthreshold regime, as shown in Fig. 3(c). Finally, the increased electron barrier reduces the electron density in the channel [23], [24]. Thus, in the subthreshold regime, I_{ds} can be reduced when V_{ds} increases for the MoS_2 NC-FETs.

Fig. 4(a) shows the simulated output characteristics against the experimental output characteristics of Dev. #2 for different V_{gs}. Note that the device works in the subthreshold region in this case. The difference between analytical model

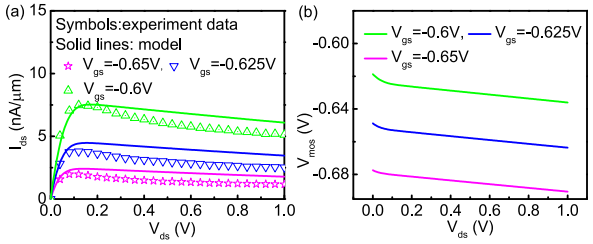

FIGURE 4. (a) Simulated output characteristics against the experiment measurement of Dev. #2 for different gate voltages. (b) Simulated the interfacial potential (V_{mos}) of the same device varying with V_{ds} for different V_{gs}.

and experimental results is likely to be caused by the simplicity of the model, which neglects polarization damping, series resistance, and field-dependent mobility. Nonetheless, experiments and simulations both show a clear signature of negative differential resistance (NDR) effect during subthreshold operation, where I_{ds} decreases with increasing V_{ds}. The NDR can be explained as follows: for a given gate voltage, V_{mos} deceases when V_{ds} increases as shown in Fig. 4(b). It is well known that V_{ds} has an negligible impact on I_{ds} of the long-channel baseline MoS_2 FET when the device works in the subthreshold region. Thus, V_{mos} dominates the drain current of the MoS_2 NC-FET. That is, the drain current reduces when V_{ds} increases. Similar NDR effects have been observed in the bulk Ge and Si NC-FETs [25], [26]. Importantly, the design parameters of the fabricated devices are not arbitrary; instead they are optimized through principle of capacitance matching to simultaneously obviate steady-state hysteresis and obtain a steep SS [27]. We focus on the long-channel 2D NC-FETs because the frequency response of these devices is limited by the damping factor of FE material and the maximum operating frequency is usually smaller than 30 MHz [28], [29].

IV. CONCLUSION

The electrical performance of back-gated 2D semiconductor NC-FETs has been investigated using both experiment and analytical modeling. Our analytical model is continuous in the entire working region (depleted region and accumulation region) of the device. We demonstrated that once optimized, 2D NC-FET could achieve sub-60 mV/dec *SS* operation over several orders of drain current at room temperature, enabled by the coupling of ferroelectric gate and parasitic capacitance. The negative DIBL and NDR effects occur naturally as consequences of this coupling effect. The 2D NC-FET model developed in this paper would help in the design and optimization of ultra-low power integrated circuits.

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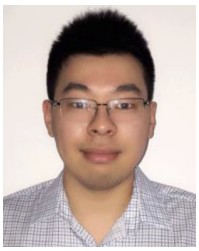
CHUNSHENG JIANG received the B.S. degree in microelectronics from Xidian University, Xi'an, China, in 2013. He is currently pursuing the Ph.D. degree in EE with Tsinghua University, Beijing, China. He is currently a visiting student with Purdue University, West Lafayette, IN, USA.

His current research interests include device physics, compact models, and circuit simulation for negative capacitance transistor and junctionless transistor.



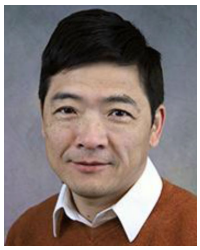
MENGWEI SI received the B.S. degree from the Department of Electronic Engineering, Shanghai Jiao Tong University, Shanghai, China, in 2012. He is currently pursuing the Ph.D. degree with the School of Electrical and Computer Engineering, Purdue University, West Lafayette, USA. His current research interests include device integration, electrical characterization and physics on high-K/III-V devices, and novel semiconductor materials.

RENRONG LIANG received the B.S. degree in microelectronics from Xidian University, Xi'an, China, in 2003 and the Ph.D. degree from Tsinghua University, Bejing, China, in 2008, where he is currently an Assistant Professor with the Institute of Microelectronics.

He currently focuses on developing novel materials, devices and related process technologies for nanoelectronics as well as exploring new materials/device physics at the nanoscale.

JUN XU received the B.S. degree in electrical engineering from Tsinghua University, Beijing, China, in 1986, and the M.S. and Ph.D. degrees in electrical engineering from the Shaanxi Institute of Microelectronics, Xi'an, China, in 1989 and 1994, respectively.

His current research interests are in general concerned with modeling, design optimization, and fabrication of SiGe/Si microwave power HBT's and high speed strained Si MOS devices and circuits.



PEIDE D. YE received the B.S. degree from Fudan University, Shanghai, China, in 1988, and the Ph.D. degree from the Max-PlanckInstitute for Solid State Research, Stuttgart, Germany, in 1996. He is currently the Mary Jo Schwartz Chair Professor of electrical and computer engineering with Purdue University, West Lafayette, IN, USA. His current research interests are high-k dielectric integration on novel channel materials including III-V, Ge, and graphene.

MUHAMMAD ASHRAFUL ALAM holds the Jai N. Gupta professorship with Purdue University, West Lafayette, IN, USA, where he focuses on the physics and technology of semiconductor devices. From 1995 to 2003, he was a Technical Staff Member with the Silicon ULSI Research Department, Bell Laboratories, Murray Hill, NJ, USA. He enjoys teaching over 100 000 students worldwide have learned some aspect of semiconductor devices from his Web-enabled courses.